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PATEL, HETUL B	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/642,862	GUPTA ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7 and 9-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 9-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on August 27, 2007. Claims 14, 27, 30 and 33-36 are amended. Claim 37 is newly added; and none of the claims are cancelled. Therefore, claims 1-2, 4-7 and 9-37 are currently pending in this application.

2. Applicant's arguments filed on August 27, 2007 have been fully considered but they are not deemed to be persuasive.

3. The rejection of claims 1-2, 4-7 and 9-36 as in the previous Office Action is respectfully maintained but updated to show the changes made by the amendment.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "said first and said second caches at least partially comprise one another" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 37 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Examiner find no support in the specification or drawing(s) of the current application for the limitation of the newly added claim 37.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4-7 and 9-36 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kashima et al. (USPN: 5,485,598) hereinafter, Kashima.

As per claim 36, Kashima teaches a method comprising

- maintaining a first cache (i.e. the disk cache 13 in Fig. 8), wherein said maintaining is performed by an upper-level system (i.e. the computer 10 in Fig. 8, especially by the CPU 11 in Fig. 8); and said first cache is configured to provide read access and write access by the upper-level system (i.e. the computer 10 in Fig. 8, especially by the CPU 11 in Fig. 8 has read and write access to the disk cache 13);
- cloning (i.e. copying) information stored in a first unit of storage (the disk cache 13 in Fig. 8) into a second unit of storage (the second cache memory 17 in Fig. 8), wherein said first cache comprises said first unit of storage and a second cache (i.e. old data cache 17 in Fig. 8) comprises said second unit of storage; and
- accessing said second cache by the other of said upper-level system and a lower-level storage module (i.e. by the disk array as described in Fig. 7 step S9) (e.g. see the abstract, Col. 5, lines 21-25 and Figs. 8 and 7); and said

second cache is configured to provide read access and write access by said other of said upper-level system and said lower-level storage module (i.e. the disk array has read and write access to the old data cache 17 in Fig. 8; see S9 and S12 in Fig. 7).

As per claim 1, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the first cache (i.e. the disk cache 13 in Fig. 4) is maintained by the upper-level system (i.e. the computer 10 in Fig. 4, especially by the CPU 11 in Fig. 4) (e.g. see the abstract and Fig. 4).

As per claim 4, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising:

- partially writing a unit of storage (i.e. a portion of data from the first cache) of a storage unit (i.e. the first cache) by writing a portion of said information (i.e. a portion of data from the first cache) from said second unit of storage (i.e. a portion of data from the second cache) to said unit of storage of said storage unit; and
- partially writing said unit of storage of said storage unit by writing new information (i.e. renewed data of the first cache) to said unit of storage of said storage unit (e.g. see the abstract).

As per claim 5, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said cloning comprises:

- reading said information (i.e. the old data of the first cache) from said first unit of storage (i.e. the first cache); and

- writing said information (i.e. the old data of the first cache) to said second unit of storage (i.e. the second cache) (e.g. see the abstract).

As per claim 6, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising writing to said first unit of storage after said reading, i.e. the old data is written/stored into the second cache after being read from the first cache (e.g. see the abstract).

As per claim 7, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising:

- reading said information (i.e. the old data) from said second unit of storage (i.e. from the second cache); and
- calculating parity information using said information, i.e. calculating new CK/parity data using the old data, the new data and the new CK data (e.g. see the abstract).

As per claim 9, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising the first unit of storage (i.e. the first cache) is to be modified if the first unit of storage is to be written to, in other words, if the first cache is written, then the first cache is modified (e.g. see the abstract).

As per claim 10, see arguments with respect to the rejection of claim 7. Claim 10 is also rejected based on the same rationale as the rejection of claim 10.

As per claims 11 and 12, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising modifying

said first unit of storage after said performing said cloning, i.e. writing new data into the first cache after copying old data from the first cache into the second cache (e.g. see the abstract).

As per claim 13, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said cloning comprising determining if said information will be needed in the future; and performing said cloning if said information will be needed in the future, i.e. if the old data is going to be renewed by the new data in the first cache, then cloning/copying process is performed since the old data may be needed in future if the new data is lost/corrupted for any reason(s) (e.g. see the abstract).

As per claim 14, Kashima teaches a storage system (shown in Fig. 4) comprising an old data cache (i.e. old data cache 17 in Fig. 8), wherein said old data cache is configured to be maintained by an upper-level system (i.e. the computer 10 in Figs. 4 and 8, especially by the CPU 11 in Figs. 4 and 8) by virtue of said old data cache being configured to provide read access and write access by said upper-level system (i.e. the computer 10 in Fig. 8, especially by the CPU 11 in Fig. 8 has read and write access to the disk cache 13), and said old data cache is further configured to be accessed by the lower-level storage module (i.e. by the disk array 2a-2d in Fig. 4 as described in S9 of Fig. 7) by virtue of said old data cache being configured to provide read access and write access by said lower-level system (i.e. the disk array has read and write access to the old data cache 17 in Fig. 8; see S9 and S12 in Fig. 7) (e.g. see the abstract and Figs. 4, 7 and 8).

As per claim 15, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising:

- the upper-level system (i.e. the computer 10 in Figs. 4 and 8) is communicatively coupled to said old data cache (i.e. 17 in Fig. 8); and
- the lower-level storage module (i.e. the disk array 2a-2d in Figs. 4 and 8), communicatively coupled to said old data cache and said upper-level system (e.g. see Figs. 4 and 8).

As per claim 16, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level storage module is a volume manager (i.e. the RAID disk array, 1 in Fig. 8).

As per claim 17, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level storage module comprises a cache (i.e. the old CK data cache, 16 in Fig. 8).

As per claim 18, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level storage module is configured to clone/copy information from a page in said cache (i.e. the old CK data cache, 16 in Fig. 8) to a page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 19, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system (i.e. the computer 10 in Fig. 4) is configured to access said page in said old data cache (i.e. 17 in Fig. 8).

As per claim 20, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system comprises a cache (i.e. the disk cache, 13 in Fig. 8).

As per claim 21, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system is configured to clone/copy information from a page in said cache (i.e. the disk cache, 13 in Fig. 8) to a page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 22, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level storage module (i.e. the disk array device, 1 in Fig. 8) is configured to access said page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 23, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system is a hardware RAID controller since RAID (i.e. 1 in Fig. 8) is controlled by the upper-level system (i.e. the computer, 10 in Fig. 8) (e.g. see Fig. 8).

As per claim 24, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising storage unit (i.e. disks, 2a-2d in Fig. 8), wherein said lower-level storage module (i.e. the disk array 2a-2d in Figs. 4 and 8) is coupled to control said storage unit (e.g. see fig. 8).

As per claim 25, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising a parity cache (i.e. the

old CK data cache, 16 in Fig. 8), wherein said storage unit is a RAID (i.e. 2a-2d in Fig. 8), and said parity cache is configured to store parity information corresponding to data read from said RAID (e.g. see the claim 18).

As per claim 26, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said storage unit (i.e. the main memory, 12 in Fig. 8) comprises a source volume (i.e. 17 in Fig. 8) and a snapshot volume (i.e. 13 in Fig. 8), and said lower-level storage module (i.e. 1 in Fig. 8) is configured to write information from a page in said old data cache (i.e. 17 in Fig. 8) to said snapshot volume (i.e. 13 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 30, Kashima teaches a storage system comprising:

- an upper-level system (i.e. the computer 10 in Fig. 8, especially by the CPU 11 in Fig. 8) comprising a first cache(i.e. the disk cache 13 in Fig. 8), wherein said first cache is configured to provide read access and write access by said upper-level system (i.e. the computer 10 in Fig. 8, especially by the CPU 11 in Fig. 8 has read and write access to the disk cache 13);
- a second cache (the second/old data cache memory 17 in Fig. 8), wherein said second cache is configured to provide read access and write access by a lower-level storage module (i.e. the disk array has read and write access to the old data cache 17 in Fig. 8; see S9 and S12 in Fig. 7);
- a processor (i.e. the CPU 11 in Fig. 8);
- computer readable medium coupled to said processor; and computer code, encoded in said computer readable medium, configured to cause said

processor to, (i.e. this feature is inherently embedded in the system taught by Kashima):

- clone/copy information stored into a first unit of storage (the first cache) into a second unit of storage (the second cache), wherein
  - said first unit of storage is stored in a first cache (i.e. 13 in Fig. 4) maintained by an upper-level system (i.e. 10 in Fig. 4), and
  - said second unit of storage is stored in a second cache (i.e. 15 in Fig. 4) configured to be accessed by a lower-level storage module (i.e. by the disk array 2a-2d in Fig. 4 as described in S9 of Fig. 7) (e.g. see Figs. 4 and 7; and the abstract).

As per claim 31, see arguments with respect to the rejection of claims 30 and 4. Claim 31 is also rejected based on the same rationale as the rejection of claims 30 and 4.

As per claim 32, see arguments with respect to the rejection of claims 30 and 5-6. Claim 32 is also rejected based on the same rationale as the rejection of claims 30 and 5-6.

As per claims 27-29, see arguments with respect to the rejection of claims 30-32, respectively. Claims 27-29 are also rejected based on the same rationale as the rejection of claims 30-32, respectively.

As per claims 33-35, see arguments with respect to the rejection of claims 30-32, respectively. Claims 33-35 are also rejected based on the same rationale as the rejection of claims 30-32, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kashima.

As per claim 2, Kashima teaches the claimed invention as described above. Furthermore, Kashima also teaches that the main memory (i.e. 12 in Fig. 8) comprise the first and second caches (i.e. 13 and 17 in Fig. 8). However, Kashima does not clearly disclose that the first and second caches are a single cache. The common knowledge or well-known in the art statement, for the prior art teaching a single cache comprising a plurality of caches, is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)). First of all, it has been held that to make integral is not generally given patentable weight. Note In re Larson 144 USPQ 347 (CCPA 1965). Furthermore In re Tomoyuki Kohno 157 USPQ 275 (CCPA 1968) states that to integrate electrical components onto a unitary, one piece structure would be obvious. Integrating multiple components on a single chip reduces cabling problems, reduces latency required for communicating among multiple components, improves efficiency of message passing, reduces chip-to-chip communications costs, allows for less pin count, area saving and high speed data transfer between the elements and leads to further

power efficiency and increased scalability. Because multiple caches integrated on a single cache (chip) provides improvements in efficiency, cost and scalability over individual caches, it would have been obvious to comprise a plurality of caches on a single cache. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

As per claim 37, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches first and second caches as two separate caches (i.e. the disk cache and old data cache, 13 and 17 in Fig. 8). However, partitioning a cache to and using them as two separate cache is well-known and notorious old in the art. Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to use a well-known partitioned cache in place of the first and second separate caches in Kashima because it reduces cabling problems, reduces latency required for communicating among caches, improves efficiency of message passing, reduces chip-to-chip communications costs (compare to if they are separate), allows for less pin count, area saving and high speed data transfer between the caches and leads to further power efficiency and increased scalability. Because partitioning a cache to create multiple caches provides improvements in efficiency, cost and scalability over individual caches, it would have been obvious to comprise a plurality of caches on a single cache. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention. Examiner herein taking Official Notice on this subject matter.

Remarks

8. As to the remark, Applicant asserted that

(a) As can be seen, the independent claims now recite that the first cache is configured to provide read access and write access by one of an upper-level system and a lower-level storage module, while the second cache is configured to provide read access and write access by the other of these modules. Nowhere is there shown, taught or suggested in Kashima that the cache(s) disclosed therein, wherein any two systems can perform read and write operations to their respective caches.

(b) Moreover, in light of these distinctions, Applicants once again respectfully submit that Kashima fails to show the cloning of the first cache into the second cache prior to modifying information in the first cache. The copying of Kashima (were such even comparable, which Applicants maintain it is not) differs markedly from the claimed cloning because neither of Kashima's first and second caches that are maintained by the upper-level system are accessible by a lower-level system (and certainly not in the claimed manner).

(c) In the Office Action, the Examiner equates the "upper-level system" of claim 36 with the CPU of Kashima, while also equating the "lower-level system" of the prior version of claim 36 with the OS of Kashima. Alternatively, the Examiner states that both the upper-level system and the lower-level system with computer 10 of Kashima. Kashima, at best, teaches a system in which the old data cache can be part of the main memory system (e.g., as shown in

Figs. 8 and 11 of Kashima) or part of a disk array (e.g., as shown in Figs. 4 and 14 of Kashima). Both the CPU and the OS are part of the computer 10. Neither the CPU nor the OS is a "lower-level storage module," as recited in the current version of claim 36. Computer 10 of Kashima is also clearly not a lower- level storage module. Accordingly, the cited art fails to teach or suggest the scenario claimed in amended claim 36, which involves a lower-level storage module maintaining or having access to a cache. And, as noted, even if such were the case (which Applicants do not concede), the read and write functionality provided by the claimed invention simply does not exist within Kashima.

(d) It is not well known to integrate caches such as those described in claim 2. Official Notice is not proper in such case, and Applicants therefore respectfully request the appropriate citation of a reference in this regard.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), Kashima does teach that the first cache is configured to provide read access and write access by the upper-level system (i.e. the computer 10 in Fig. 8, especially by the CPU 11 in Fig. 8) has read and write access to the disk cache 13); and the second cache is configured to provide read access and write access by said other of said upper-level system and said lower-level storage module (i.e. the disk array has read and write access to the old data cache 17 in Fig. 8; see S9 and S12 in Fig. 7).

With respect to (b), Kashima does disclose about cloning (i.e. copying) information stored in a first unit of storage (the disk cache 13 in Fig. 8) into a second unit of storage (the second cache memory 17 in Fig. 8), wherein said first cache comprises said first unit of storage and a second cache (i.e. old data cache 17 in Fig. 8) comprises said second unit of storage (e.g. see Col. 5, lines 21-26 and S10 in Fig. 8). Furthermore, the copying of Kashima is similar to the claimed cloning because Kashima's second cache (i.e. 17 in Fig. 8) that is maintained by the upper-level system (i.e. the computer 10 in Fig. 8, especially by the CPU 11 in Fig. 8) is accessible by a lower-level system (i.e. the disk array) (see S9 and S12 in Fig. 7).

With respect to (c), Examiner is not equating the claimed limitations with Kashima's teachings as alleged by Applicant in this argument. Kashima does clearly teach each and every limitations of claims 1, 4-7 and 9-36 as described above in the rejection of them.

With respect to (d), the common knowledge or well-known in the art statement, for the prior art teaching a single cache comprising a plurality of caches, is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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